[0020] FIG. **7** is a chart showing an angle at a standing up, an on-resistance and a breakdown voltage of MOSFETs according to Example 2-1, 2-2 and Comparative example 2, respectively;

[0021] FIG. **8** is a cross sectional view showing an MOSFET according to a fourth embodiment;

[0022] FIGS. **9**A to **9**D are views showing one example of a process for producing the MOSFET shown in FIG. **8**; and

[0023] FIG. **10** is a chart showing an angle at a standing up, an on-resistance and a breakdown voltage regarding individual MOSFETs according to Example 3-1, 3-2 and Comparative example 3, respectively.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0024] Embodiments of a field effect transistor and of a process for producing the field effect transistor according to the present invention will be described in detail below with reference to the drawings. The present invention is not limited to the embodiments.

[0025] FIG. **1** is a cross sectional view showing exemplary an MOSFET according to a first embodiment of the present invention. In the MOSFET **100**, there are formed an AlN layer **102**, a buffer layer **103** formed by laminating alternately a GaN layer and an AlN layer, and a lower part semiconductor layer **104** comprised of p-GaN on a substrate **101** comprised of sapphire, SiC, Si, or the like. A semiconductor operating layer **105** is formed on the lower part semiconductor layer **104**. Regarding the semiconductor operating layer **105**, a carrier drifting layer **105***a*, which is comprised of undope GaN, and a carrier supplying layer **105***b*, which is comprised of n-AlGaN and has a band gap energy different from that of the carrier drifting layer **105***a*, are laminated one by one. A recess part **105***c* is formed by removing a part of the carrier drifting layer **105***a* and of the carrier supplying layer **105***b* to a depth reaching the lower part semiconductor layer **104**. On the semiconductor operating layer **105**, a source electrode **106** and a drain electrode **107** are formed and sandwich the recess part **105***c*. A gate insulating layer **108**, which is comprised of SiO_2 or the like, is formed over a top surface of the semiconductor operating layer **105** and a top surface **104***a* of the lower part semiconductor layer **104** at an inside of the recess part **105***c*. At the recess part **105***c*, a gate electrode **109** is formed on the gate insulating layer **108**.

[0026] The MOSFET **100** is operated as a normally off type. Due to a two dimensional electron gas generated at an interface of the carrier drifting layer **105***a* to the carrier supplying layer **105***b*, it becomes able to obtain a low on-resistance and a faster switching operation.

[0027] In the MOSFET **100**, a side wall **105***d* at a side of the drain electrode **107** of the recess part **105***c* stands up with inclining at an angle of θ**1** from the top surface **104***a* of the lower part semiconductor layer **104**. Accordingly, it is possible to alleviate a localized convergence of an electric field between the gate and the drain, as opposed to the conventional configuration where a side wall stands up vertically from a surface of a lower part semiconductor layer. As a result, it becomes able to obtain the MOSFET **100** having a high breakdown voltage.

[0028] In the MOSFET **100**, the side wall **105***d* is inclined, so that a thickness of the carrier supplying layer **105***b* decreases gradually from a side of the drain electrode **107**. Therefore, a density of the two dimensional electron gas to be generated at the carrier drifting layer **105***a* decreases gradually corresponding to the decrease in the thickness of the carrier supplying layer **105***b*. As a result, a reduced surface field (RESURF) region is formed directly under the gate electrode **109** for alleviating the local convergence of the electric field, thereby further improving the breakdown voltage.

[0029] When the angle θ**1** is less than 90 degrees, it is able to relax the localized convergence of the electric field. It is preferable the angle θ**1** is smaller than 75 degrees, and more preferably is not smaller than 65 degrees, because it is able to relax the localized convergence sufficiently. When the angle of θ**1** is greater than 30 degrees, the on-resistance reduces, and a distance between the source and the drain becomes too long, thereby making it desirable to reduce a size for a device and a producing cost.

[0030] In the MOSFET **100**, a side wall **105***e* at a side of the source electrode **106** of the recess part **105***c* stands up as well, with inclining at an angle θ**2** from the top surface **104***a* of the lower part semiconductor layer **104**. The angle θ**2** is similar to the angle θ**1**. However, regarding the side wall **105***e*, the angle θ**2** may be different from the angle θ**1**, and the side wall **105***e* may stand up vertically from the top surface **104***a*.

[0031] Next, a process for producing the MOSFET **100** will be described in detail below. FIGS. **2**A to **2**F are explanatory views explaining one example of the process for producing the MOSFET **100**. In the following description, a metalorganic chemical vapor deposition (MOCVD) method is used, and the invention is not limited thereto.

[0032] First, as shown in FIG. **2**A, the substrate **101** comprised of Si and having an (111) plane as a principal top surface plane is set to an MOCVD device. Next, using a hydrogen gas with a concentration of 100% as a carrier gas, trimethylgallium (TMGa), trimethylaluminum (TMAl) and NH_3 are introduced at a flow rate of 58 μmol/min, 100 μmol/min and 12 l/min, respectively. Then, the lower part semiconductor layer **104** comprised of the AlN layer **102**, the buffer layer **103** and the p-GaN is epitaxially grown on the substrate **101** one by one to be at a growth temperature of 1,050° C. As a doping source of p-type corresponding to the lower part semiconductor layer **104**, biscyclopentadienylmagnesium (Cp2Mg) is used. A flow rate of Cp_2Mg is controlled such that a concentration of Mg becomes approximately 1×10^{17} cm^{-3}. Next, TMGa and NH_3 are introduced at a flow rate of 19 μmol/min and 12 l/min, respectively. The carrier drifting layer **105***a* comprised of an undope GaN is epitaxially grown on the lower part semiconductor layer **104** at a growth temperature of 1,050° C. Then, TMAl, TMGa and NH_3 are introduced at a flow rate of as 125 μmol/min, 19 μmol/min, and 12 l/min, respectively. Then, the carrier supplying layer **105***b* comprised of n-AlGaN having an Al composition of 25% is epitaxially grown on the carrier drifting layer **105***a*, thereby forming the semiconductor operating layer **105**. SiH_4 is used as a doping source of n type for the carrier supplying layer **105***b*.

[0033] In the above description, the buffer layer **103** is formed of approximately eight layers of a GaN/AlN composite lamination having a thickness of 200/20 nm. The thicknesses of the AlN layer **102**, the lower part semiconductor layer **104**, the carrier drifting layer **105***a*, and the carrier supplying layer **105***b* are 100 nm, 500 nm, 100 nm, and 20 nm, respectively.

[0034] Next, as shown in FIG. **2**B, using a plasma chemical vapor deposition (PCVD) method, a mask layer **110** comprised of amorphous silicon (a-Si) is formed on the carrier